



Product Specification

M190EP02 V2

AU OPTRONICS CORPORATION

(V) Preliminary Specification

() Final Specification

Module	19.0" SXGA Color TFT-LCD
Model Name	M190EP02 V2

<table><tr><td>Customer</td><td>Date</td></tr><tr><td> </td><td> </td></tr><tr><td>Approved by</td><td></td></tr><tr><td> </td><td> </td></tr></table>	Customer	Date			Approved by				<table><tr><td>Checked & Approved by</td><td>Date</td></tr><tr><td><u>CC Chiu</u></td><td><u>May. 2, 2006</u></td></tr><tr><td>Prepared by</td><td></td></tr><tr><td><u>Jack CC Hsu</u></td><td><u>May. 2, 2006</u></td></tr></table>	Checked & Approved by	Date	<u>CC Chiu</u>	<u>May. 2, 2006</u>	Prepared by		<u>Jack CC Hsu</u>	<u>May. 2, 2006</u>
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Record of Revision

Version & Date		Page	Old Description	New Description	Remark
0.1	2006/05/02	All	First Edition for Customer	-	



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1. Handling Precautions

- 1) Since front polarizer is easily damaged, pay attention not to scratch it.
- 2) Be sure to turn off power supply when inserting or disconnecting from input connector.
- 3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
- 4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
- 5) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface.
- 6) Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.
- 7) Do not open or modify the Module Assembly.
- 8) Do not press the reflector sheet at the back of the module to any directions.
- 9) In case if a Module has to be put back into the packing container slot after once it was taken out from the container, do not press the center of the CCFL reflector edge. Instead, press at the far ends of the CCFL Reflector edge softly. Otherwise the TFT Module may be damaged.
- 10) At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the Interface Connector of the TFT Module.
- 11) After installation of the TFT Module into an enclosure, do not twist nor bend the TFT Module even momentary. At designing the enclosure, it should be taken into consideration that no bending/twisting forces are applied to the TFT Module from outside. Otherwise the TFT Module may be damaged.
- 12) Cold cathode fluorescent lamp in LCD contains a small amount of mercury. Please follow local ordinances or regulations for disposal.
- 13) Small amount of materials having no flammability grade is used in the LCD module. The LCD module should be supplied by power complied with requirements of Limited Power Source (IEC60950 or UL1950), or be applied exemption.
- 14) The LCD module is designed so that the CCFL in it is supplied by Limited Current Circuit (IEC60950 or UL1950). Do not connect the CCFL in Hazardous Voltage Circuit.



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2. General Description

M190EP02 is a Color Active Matrix Liquid Crystal Display composed of a TFT-LCD panel, a driver circuit, and backlight system. The screen format is intended to support the SXGA (1280(H) x 1024(V)) screen and 16.2M colors (RGB 6-bits + FRC data). All input signals are Analog RGB interface compatible, DVI interface optional. Inverter card of backlight is not included. M190EP02 is designed for a display unit of personal computer.

2.1 Display Characteristics

The following items are characteristics summary on the table under 25 °C condition:

Items	Unit	Specifications
Screen Diagonal	[mm]	482.6 (19.0")
Active Area	[mm]	376.320(H) × 301.060(V)
Pixels H x V		1280 × 3(RGB) × 1024
Pixel Pitch	[mm]	0.294(per one triad) × 0.294
Pixel Arrangement		R.G.B. Vertical Stripe
Display Mode		Normally White
White Luminance	[cd/m ²]	250 (Typ) ¹
Contrast Ratio		700 : 1 (Typ)
Optical ResponseTime	[msec]	6ms(Typ, on/off) ; 2ms(AVG., GTG)
Nominal Input Voltage VCC	[Volt]	+5.0 (Typ)
Power Consumption	[Watt]	30.6 W (Typ) ; 0.4 W (Stand by)
Weight	[Grams]	2500 (Typ)
Physical Size (H x V x D)	[mm]	396.0(H) x 324.0(V) x 21.7(D) (Typ)
Electrical Interface		VESA standard Analog RGB and DVI 1.0
Surface Treatment		Anti-glare type, Harness 3H
Support Color		16.2M colors (RGB 6-bits + FRC data)
Plug & Play		VESA DDC1/2B/2Bi/2B+/CI ²
Compability		PC/MAC
Max. Firmware Code Size	[bit]	128K
Max. Pixel Clock	[MHz]	135.09 MHz
6500K White Point (CIE x,y)		(0.313,0.329) +/-0.03 ²
Auto Adjustment		Auto Color, Size & Phase ²
Temperature Range Operating Storage (Non-Operating)	[°C] [°C]	0 to +50 -20 to +60
RoHS Compliance		RoHS Compliance
TCO '03 Compliance		TCO '03 Compliance ³

¹ At CCFL= 7.5 mA

² With AUO standard firmware

³ With AUO standard power module & firmware



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2.2 Optical Characteristics

The optical characteristics are measured under stable conditions at 25°C (Room Temperature):

Item	Unit	Conditions	Min.	Typ.	Max.	Note
Viewing Angle	[degree]	Horizontal (R+L) CR = 10	140	160	-	1
		Vertical (U+D) CR = 10	140	160	-	
Luminance Uniformity	[%]	9 Points	75	80	-	2, 3
Optical Response Time	[msec]	Rising	-	4.5	7	4, 6
		Falling	-	1.5	2	
		Rising + Falling	-	6	9	
		Grey to Grey (Avg.)	-	2	-	6
Color / Chromaticity Coordinates (CIE 1931)		Red x	0.61	0.64	0.67	4
		Red y	0.31	0.34	0.37	
		Green x	0.26	0.29	0.32	
		Green y	0.58	0.61	0.64	
		Blue x	0.11	0.14	0.17	
		Blue y	0.04	0.07	0.10	
		White x	0.28	0.31	0.34	
		White y	0.30	0.33	0.36	
White Luminance (At CCFL= 7.5mA)	[cd/m ²]		200	250	-	4
Contrast Ratio			500	700	-	4
Cross Talk (At 75Hz)	[%]		-	-	1.5	5
Flicker	[dB]		-	-	-20	7

Optical Equipment: BM-5A, BM-7, PR880, or equivalent



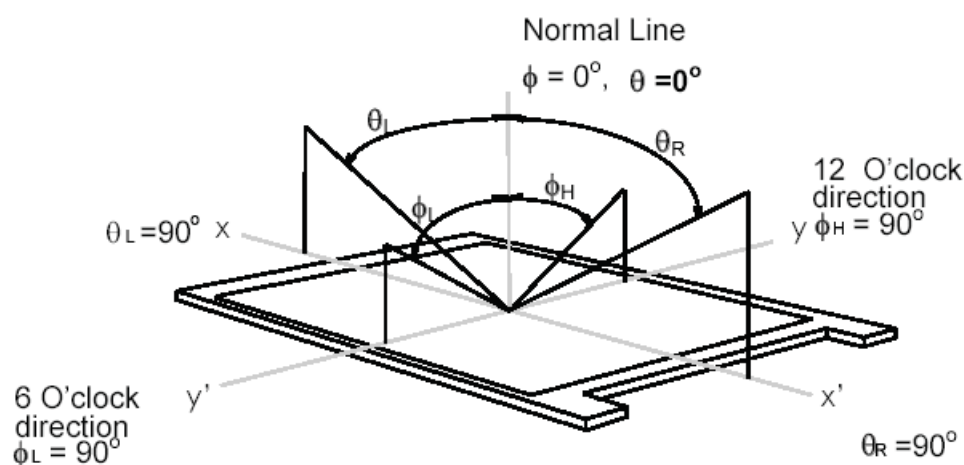
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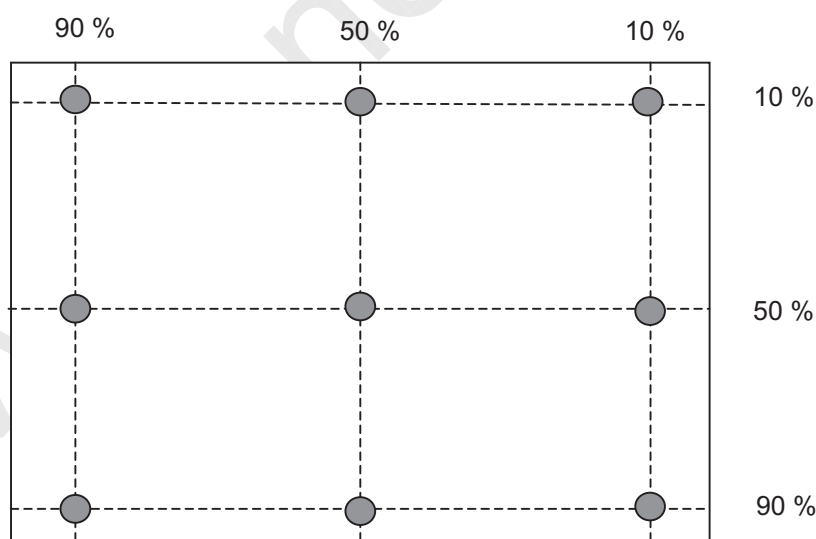
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Note 1: Definition of viewing angle

Viewing angle is the measurement of contrast ratio ≥ 10 , at the screen center, over a 180° horizontal and 180° vertical range (off-normal viewing angles). The 180° viewing angle range is broken down as follows; 90° (θ) horizontal left and right and 90° (Φ) vertical, high (up) and low (down). The measurement direction is typically perpendicular to the display surface with the screen rotated about its center to develop the desired measurement viewing angle.



Note 2: 9 points position



Note 3: The luminance uniformity of 9 points is defined by dividing the maximum luminance values by the minimum test point luminance

$$\delta_{w9} = \frac{\text{Minimum Luminance of 9 points}}{\text{Maximum Luminance of 9 points}}$$



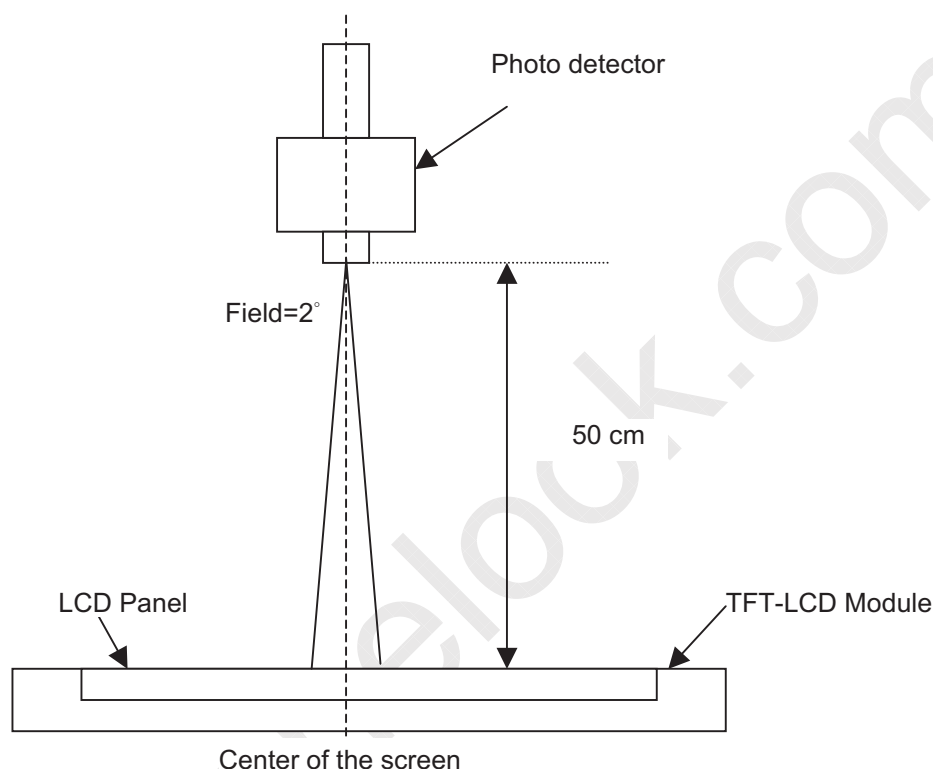
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Note 4: Measurement method

The LCD module should be stabilized at given temperature for 30 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 30 minutes in a stable, windless and dark room.



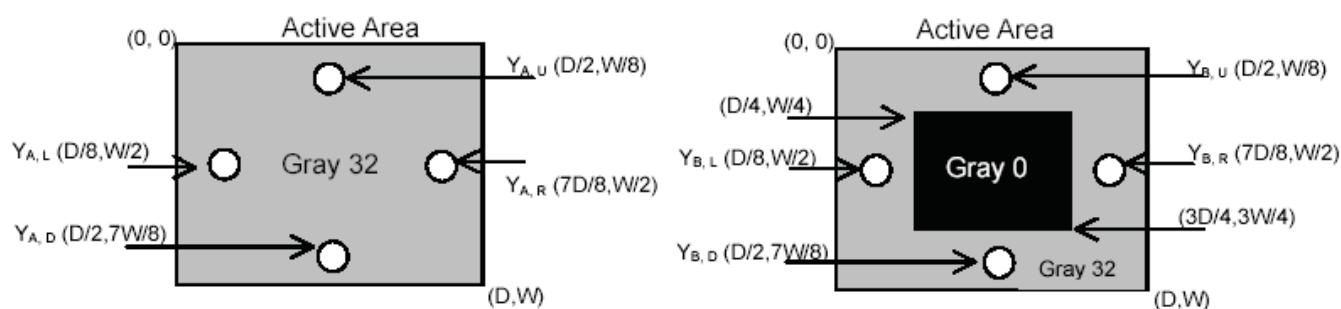
Note 5: Definition of Cross Talk (CT)

$$CT = |YB - YA| / YA \times 100 (\%)$$

Where

YA = Luminance of measured location without gray level 0 pattern (cd/m2)

YB = Luminance of measured location with gray level 0 pattern (cd/m2)





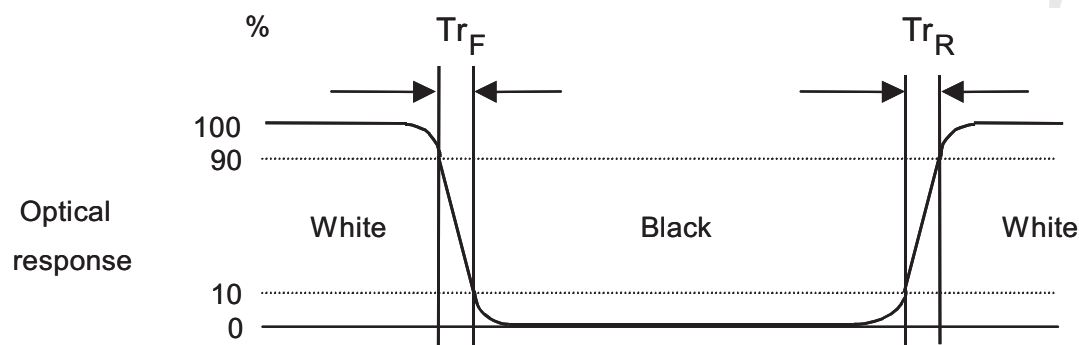
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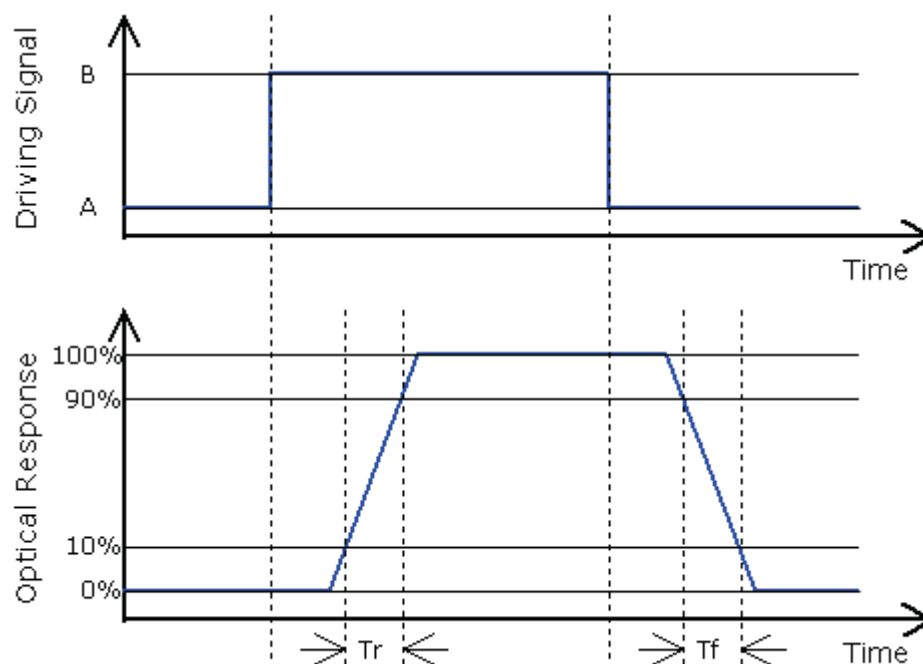
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Note 6: Definition of response time:

The output signals of photo detector are measured when the input signals are changed from “Full Black” to “Full White” (rising time), and from “Full White” to “Full Black ”(falling time), respectively. The response time is interval between the 10% and 90% of amplitudes. Please refer to the figure as below.



Over-Drive and Response time:



Algorithm:

$| \text{Level A} - \text{Level B} | \geq 32$ then the average of Grey-to-Grey response time is 2 ms. (F= 60 Hz).

T_r (rising time; from “Black” to “White”) + T_f (Falling time; from “White” to “Black”) = 6 ms(typ).

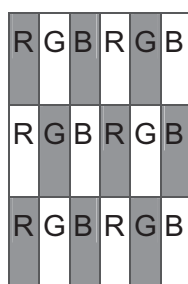


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Note 7: Subchecker Pattern

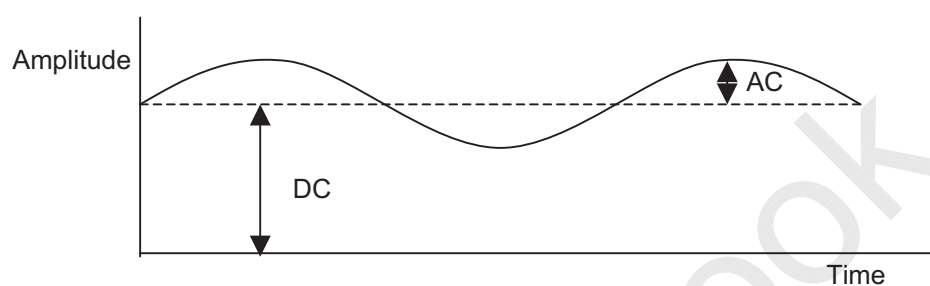


Gray Level = L127



Gray Level = L0

Method: Record dBV & DC value with (WESTAR)TRD-100



$$\text{Flicker (dB)} = 20 \log \frac{\text{AC Level(at 30 Hz)}}{\text{DC Level}}$$



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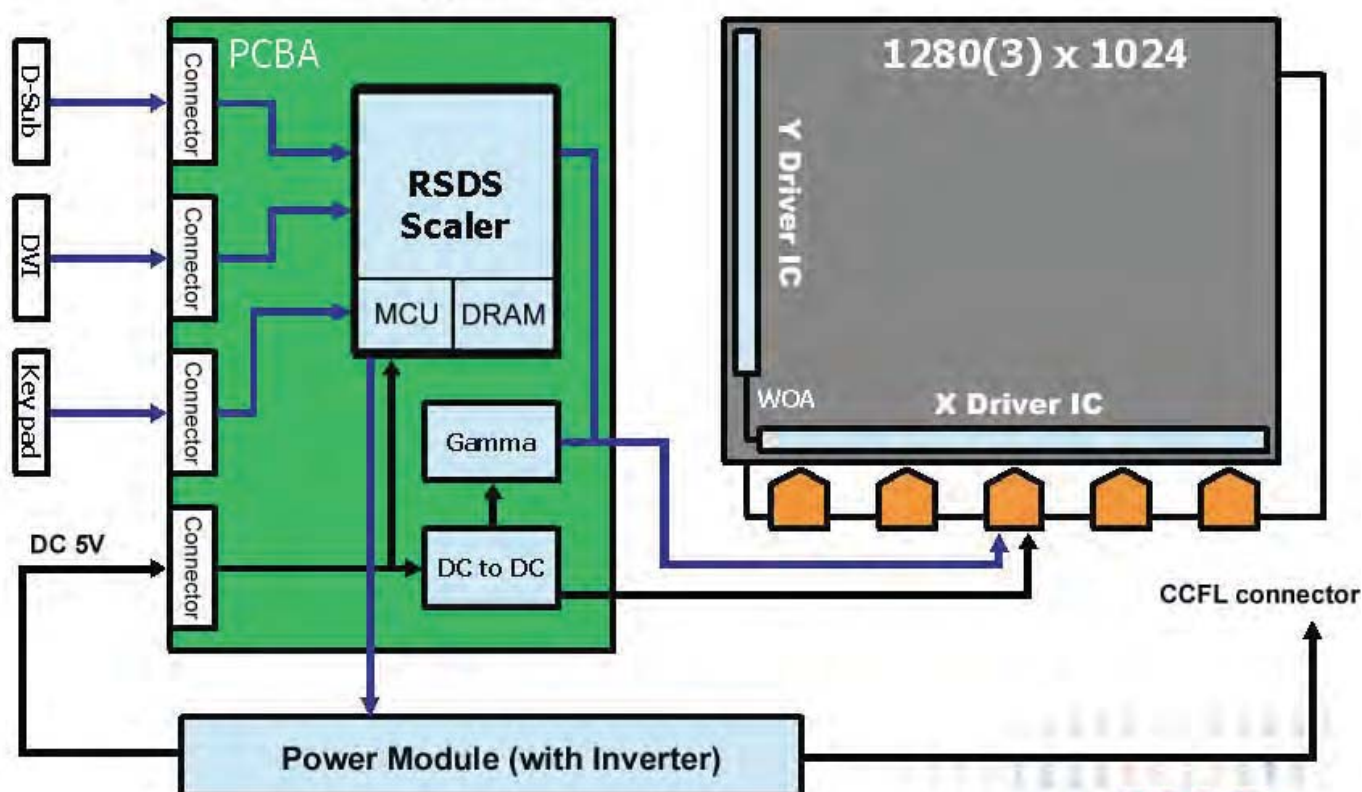
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3. Functional Block Diagram

The following diagram shows the functional block of the 19.0 inches Color TFT-LCD Module:

Block Diagram





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4. Absolute Maximum Ratings

Absolute maximum ratings of the module is as following:

4.1 Absolute Ratings of TFT LCD Module

Item	Symbol	Min.	Max.	Unit	Conditions
Logic/LCD Drive Voltage	VCC	-0.3	+5.25	[Volt]	Note 1, 2

4.2 Absolute Ratings of Backlight Unit

Item	Symbol	Min.	Max.	Unit	Conditions
CCFL Current	ICFL	0	8.5	[mA] rms	Note 1, 2

4.3 Absolute Ratings of Environment

Item	Symbol	Min.	Max.	Unit	Conditions
Operating Temperature	TOP	0	+50	[°C]	Note 3
Operation Humidity	HOP	5	90	[%RH]	
Storage Temperature	TST	-20	+60	[°C]	
Storage Humidity	HST	5	90	[%RH]	



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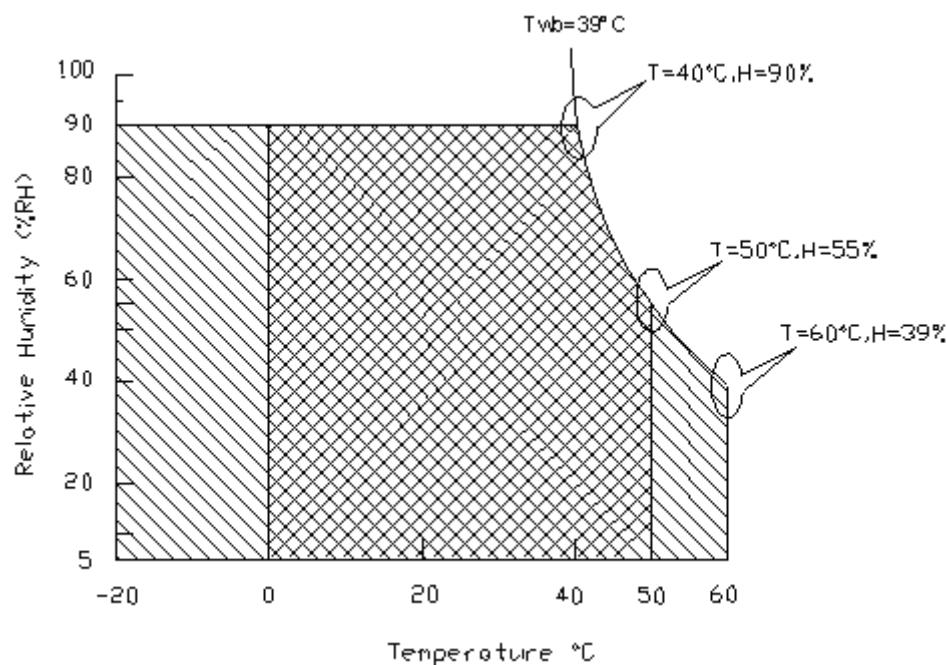
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Note 1: With in $T_a = 25^{\circ}\text{C}$

Note 2: Permanent damage to the device may occur if exceed maximum values

Note 3: For quality performance, please refer to AUO IIS (Incoming Inspection Standard).



Operating Range



Storage Range





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5. Electrical characteristics

5.1 TFT LCD Module

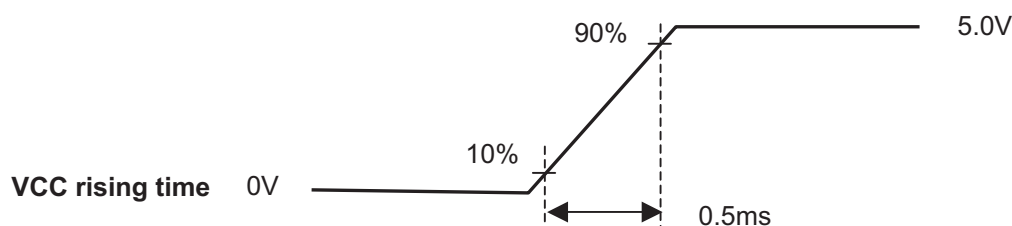
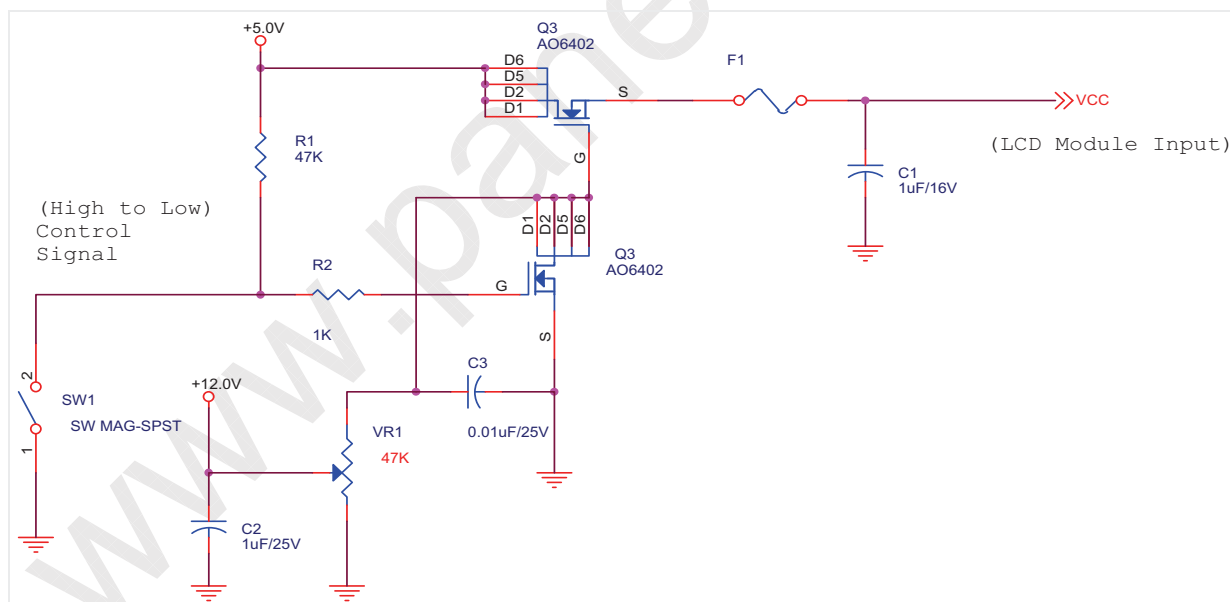
5.1.1 Power Specification

Input power specifications are as follows:

Symble	Parameter	Min.	Typ.	Max.	Unit	Condition
VCC	Logic/LCD Drive Voltage	4.75	5.0	5.25	[Volt]	Load Capacitance 20uF
ICC	Input Current	-	1.8	1.81	[A]	VCC= 5.0V, All Black Pattern
PCC	VCC Power	-	9	9.5	[Watt]	Note 1, VCC= 5.0V, All Black Pattern
IRush	Inrush Current	-	-	3.0	[A]	Note 2
VCCrp	Allowable Logic/LCD Drive Ripple Voltage	-	-	100	[mV] p-p	
PS	Power Saving	-	0.4	0.5	[Watt]	VCC= 5.0V

Note 1: The variance of VCC power consumption is $\pm 10\%$.

Note 2: Measurement conditions:





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5.2 Backlight Unit

Parameter guideline for CCFL Inverter is under stable conditions at 25°C (Room Temperature):

Parameter	Min.	Typ.	Max.	Unit	Condition
CCFL Standard Current(ISCFL)	7.0	7.5	8.0	[mA] rms	Note 2
CCFL Operation Current(IRCFL)	3.0	7.5	8.0	[mA] rms	Note 2
CCFL Frequency(FCFL)	40	60	80	[KHz]	Note 3,4
CCFL Ignition Voltage(ViCFL, Ta= 0°C)	1500	-	-	[Volt] rms	Note 5
CCFL Ignition Voltage(ViCF, Ta= 25°C)	1160	-	-	[Volt] rms	
CCFL Operation Voltage (VCFL)	-	720 (@ 7.5mA)	845 (@ 3.0mA)	[Volt] rms	Note 6
CCFL Power Consumption(PCFL)	-	21.60	23.76	[Watt]	Note 6
CCFL Life Time(LTCFL)	40,000	50,000	-	[Hour]	

Note 1: Typ. are AUO recommended design points.

- *1 All of characteristics listed are measured under the condition using the AUO test inverter.
- *2 In case of using an inverter other than listed, it is recommended to check the inverter carefully. Sometimes, interfering noise stripes appear on the screen, and substandard luminance or flicker at low power may happen.
- *3 In designing an inverter, it is suggested to check safety circuit very carefully. Impedance of CCFL, for instance, becomes more than 1 [M ohm] when CCFL is damaged.
- *4 Generally, CCFL has some amount of delay time after applying kick-off voltage. It is recommended to keep on applying kick-off voltage for 1 [Sec] until discharge.
- *5 Reducing CCFL current increases CCFL discharge voltage and generally increases CCFL discharge frequency. So all the parameters of an inverter should be carefully designed so as not to produce too much leakage current from high-voltage output of the inverter.

Note 2: It should be employed the inverter which has "Duty Dimming", if IRCFL is less than 4mA.

Note 3: CCFL discharge frequency should be carefully determined to avoid interference between inverter and TFT LCD.

Note 4: The frequency range will not affect to lamp life and reliability characteristics.

Note 5: CCFL inverter should be able to give out a power that has a generating capacity of over 1,500 voltage. Lamp units need 1,500 voltage minimum for ignition.

Note 6: The variance of CCFL power consumption is $\pm 10\%$. Calculator value for reference (ISCFL $\times$ VCFL $\times$ 4 = PCFL)



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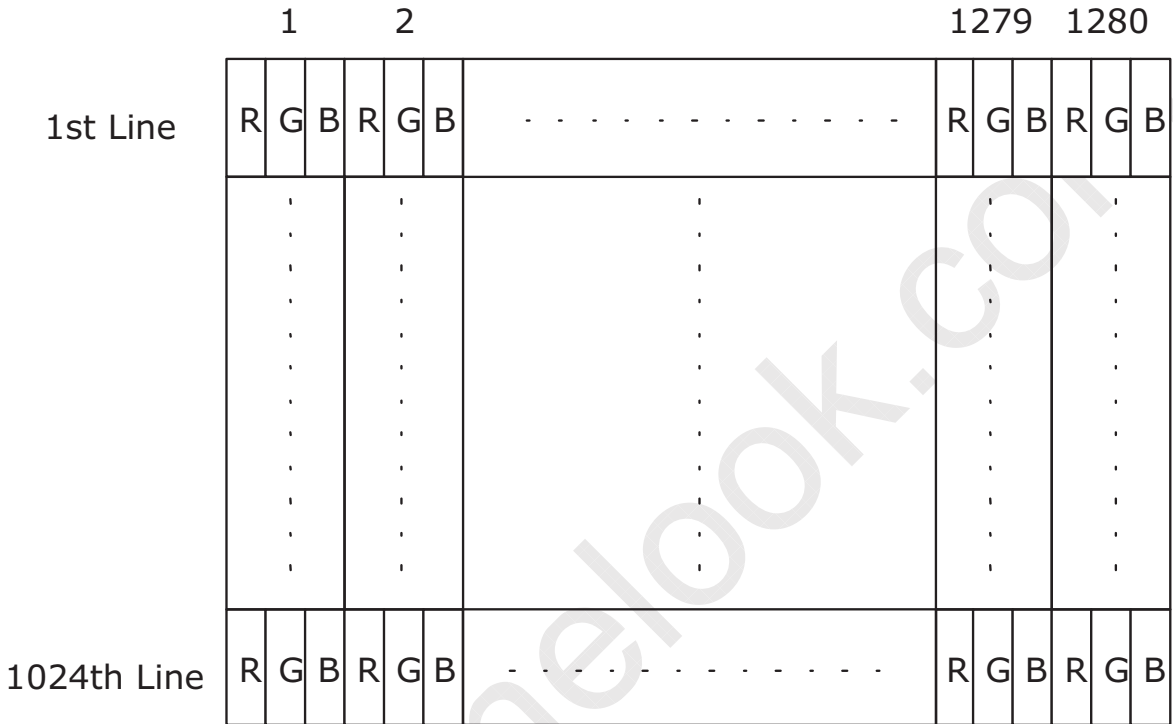
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6. Signal Characteristic

6.1 Pixel Format Image

Following figure shows the relationship of the input signals and LCD pixel format.





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6.2 Signal Description

The LVDS receiver equipped in this LCD module is compatible with SN75LVDS86 standard. LVDS is a differential signal technology for LCD interface and high speed data transfer device. Transmitter shall be SN75LVDS84 (negative edge sampling) or compatible.

➤ Power Connector (J1)

PIN#	Signal Name	Description
1	VCC	DC 5V
2	VCC	DC 5V
3	GND	Ground
4	GND	Ground
5	NC	NC
6	GND	Ground
7	BKLT_ADJ	Light adjust for the DC/AC inverter(PWM)
8	BKLT_EN	Enable for the DC/AC inverter
9	AUDIO_EN	Enable audio power control signal
10	MUTE	Mute audio
11	VOLUME	Adjust audio volume(PWM)
12	GND	Ground



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➤ VGA Connector (J2)

PIN#	Signal Name	Description
1	GND	Ground
2	VS	Vsync input from VGA host
3	HS	Hsync input from VGA host
4	GNDB	Ground for the video blue signal
5	BIN	Video blue signal
6	GNDG	Ground for the video green signal
7	GIN	Video green signal
8	GNDR	Ground for the video red signal
9	RIN	Video red signal
10	GND	Ground
11	SDA	Data signal for the DDC2B
12	SCL	Clock signal for the DDC2B
13	PC5V	DC 5V from the PC host
14	VGA_CON	Video cable connected detect signal(host connect this pin to ground)

➤ OSD Connector (J4)

PIN#	Signal Name	Description
1	GND	Ground
2	SOURCE	OSD item source function.
3	SELECT	OSD item select function.
4	LED_G	LED Green for the full mode.
5	LED_A	LED Amber for the sleep mode.
6	UP	OSD up selection function.
7	DOWN	OSD down selection function.
8	MINUS	OSD minus selection function.
9	PLUS	OSD plus selection function.
10	MENU	OSD menu on/off function.
11	Power	Power on/off function.
12	NC	
13	GND	Ground



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➤ DVI Connector (J3)

PIN#	Signal Name	Description
1	GND	Ground
2	GND	Ground
3	RX2+	TMDS RX2+ signal
4	DVI_5V	DC 5V from the PC host
5	RX2-	TMDS RX2- signal
6	HPD	Host detect for the DVI
7	GND	Ground
8	GND	Ground
9	RX1+	TMDS RX1+ signal
10	SDA	Data signal for the DDC2B
11	RX1-	TMDS RX1- signal
12	SCL	Clock signal for the DDC2B
13	GND	Ground
14	GND	Ground
15	RX0+	TMDS RX0+ signal
16	NC	
17	RX0-	TMDS RX0- signal
18	NC	
19	GND	Ground
20	GND	Ground
21	RXC+	TMDS RXC+ signal
22	DVI_CON	DVI cable connected detect
23	RXC-	TMDS RXC- signal
24	GND	Ground
25	GND	Ground
26	NC	
27	NC	
28	GND	Ground
29	GND	Ground
30	NC	



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6.3 The input data format

The input data format is followed the VESA Vedio Signal Standard. In each RGB termination is described as following table.

	Values
Max Luminance Voltage Input Data = (FFh)	0.700 Volts +0.070 /-0.035 volts
Min Luminance voltage Input Data = (00h)	0.000 Volts
Video Channel Rise/Fall Time Max	25% of minimum pixel clock period
Maximum Settling Time after overshoot/undershoot	30% of minimum pixel clock period averaged over 100 waveforms to 5% final full-scale value.
Monotonic	Yes
Resolution	1 LSB
Integral Linearity Error	± 1 LSB
Differential Linearity Error	± 1 LSB
Video Channel to Video Channel Mismatch	6% of any video output voltage over the full voltage range
Video Noise injection ratio	± 2.5 % of Max Luminance Voltage
Video Channel to Video Channel Output Skew	50% of minimum pixel clock period
Overshoot/Undershoot	±12% of step function voltage level over the full voltage range



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The Synchronization (Hsync and Vsync) Signal format is described as following table.

	Min.	Max.
Driver Logic Level "1"	2.4 Volts	5.5 Volts
Driver Logic Level "0"	0.0 Volts	0.5 Vots
Driver High Level Output Current	8mA	
Driver Low Level Output Current	8mA	
Receiver Logic Level "1"	2.0 Volts	
Receiver Logic Level "0"		0.8 Volts
Fall Time Max		80% of minimum pixel clock period
Rise Time Max		80% of minimum pixel clock period
Monotonic Rise/Fall Voltage range	0.5-2.4 Volts	
Overshoot/Undershoot		30% of high level signal voltage range No signal excursions allowed in the 0.5-2.4 volt voltage range
Jitter (Measured between Hsync pulses)		Over the frequency spectrum: One half of the difference between the maximum and minimum interval between Hsync pulses measured over 100,000 intervals shall be less than 15% of the pixel clock, 0Hz to max. horizontal refresh rate at all image formats, worst-case screen patterns.

✧ LSB: Least Significant Bit

✧ Monotonic

1. The property of either never increasing or never decreasing in reference to the slope of a transient response.
2. A constant slope value containing no inflection points.

✧ Sync: Synchronization Signals

For more details, please refer to VESA (**Video Electronics Standards Association**) Video Signal Standard.



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6.4 Signal Electrical Characteristics

➤ Power interface

Pin#	Name	Type	Min.	Typ.	Max.	Unit	Remark
1	VCC		4.75	5.0	5.25	V	1.5A
2	VCC		4.75	5.0	5.25	V	
3	GND						
4	GND						
5	NC						
6	GND						
7	BKLT_ADJ	High (Max.)		VCC		V	Internal serial 3.2K Ohm
		Low (Min.)		0.3		V	Internal serial 2.2K Ohm
8	BKLT_EN	High (On)		VCC		V	Internal serial 1K Ohm
		Low (Off)		0.3		V	
9	AUDIO_EN	High (On)	2.65		3.3	V	-4mA
		Low (Off)	GND		0.45	V	5mA
10	MUTE	High (On)	2.65		3.3	V	-4mA
		Low (Off)	GND		0.45	V	5mA
11	VOLUME	High (Max.)	3.2			V	
		Low (Min.)			0.1	V	4mA
12	GND						



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➤ VGA interface

Pin#	Name	Type	Min.	Typ.	Max.	Unit
1	GND					
2	VS	High	2.5		VCC	V
		Low	GND		0.8	
3	HS	High	2.5		VCC	V
		Low	GND		0.8	
4	GNDB					
5	BIN			700		mV
6	GNDG					
7	GIN			700		mV
8	GNDR					
9	RIN			700		mV
10	GND					
11	SDA	High	3.5		VCC	V
		Low	GND		0.8	V
12	SCL	High	3.5		VCC	V
		Low	GND		0.8	V
13	PC5V					
14	VGA_CON					



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➤ OSD interface

Pin#	Name	Type	Min.	Typ.	Max.	Unit
1	GND					
2	SOURCE	High	2.65		3.3	V
		Low	0		0.45	V
3	SELECT	High	2.65		3.3	V
		Low	0		0.45	V
4	LED_G				3.3	
5	LED_A				3.3	
6	UP	High	2.65		3.3	V
		Low	0		0.45	V
7	DOWN	High	2.65		3.3	V
		Low	0		0.45	V
8	MINUS	High	2.65		3.3	V
		Low	0		0.45	V
9	PLUS	High	2.65		3.3	V
		Low	0		0.45	V
10	MENU	High	2.65		3.3	V
		Low	0		0.45	V
11	Power	High	2.65		3.3	V
		Low	0		0.45	V
12	NC					
13	GND					



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6.5 Interface Timings

The signal interface of the TFT-LCD module is analog RGB compatible.

6.5.1 Timing Characteristics

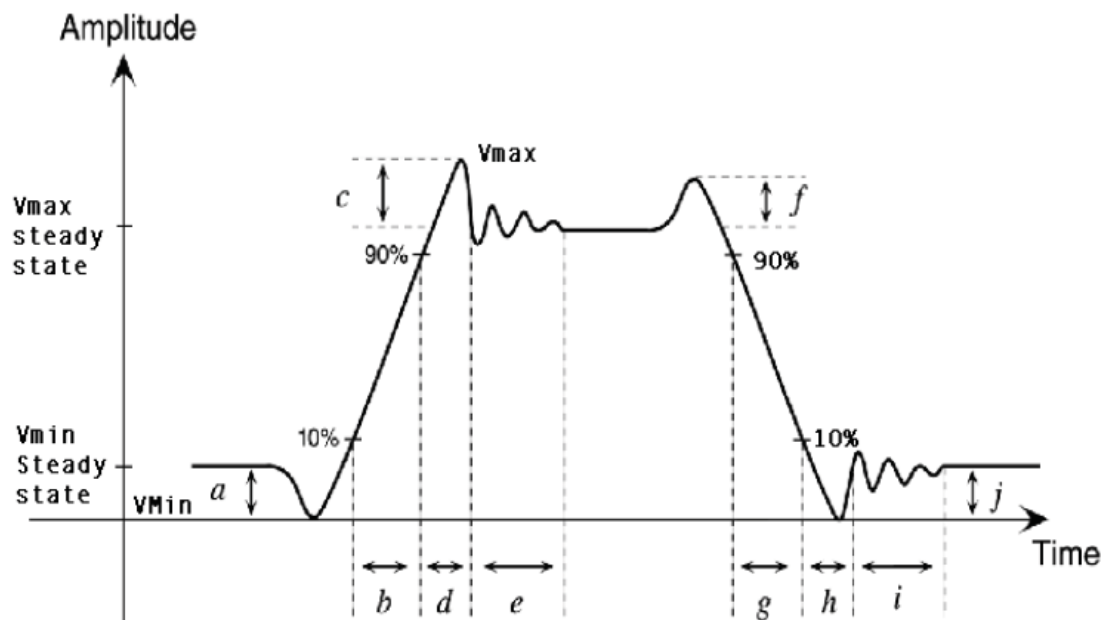
The timings are supported by the signal interface of M190EP02 are listed as following table.

Resolution	Horizontal Frequency (KHz)	Vertical Frequency (Hz)	Dot Clock (MHz)	Actually Display Resolution	Remark
640x350	31.47(P)	70.08(N)	25.17	1280x943	DOS
720x400	31.47(N)	70.08(P)	28.32	1280x1024	DOS
640x480	31.47(N)	60.00(N)	25.18	1280x1024	DOS
640x480	35.00(N)	67.00(N)	30.24	1280x1024	Macintosh
640x480	37.86(N)	72.80(N)	31.5	1280x1024	VESA
640x480	37.50(N)	75.00(N)	31.5	1280x1024	VESA
800x600	37.88(P)	60.32(P)	40	1280x1024	VESA
800x600	48.08(P)	72.19(P)	50	1280x1024	VESA
800x600	46.86(P)	75.00(P)	49.5	1280x1024	VESA
832X624	49.72(N)	74.55(N)	57.29	1280x1024	Macintosh
1024x768	48.36(N)	60.00(N)	65	1280x1024	VESA
1024x768	56.48(N)	70.10(N)	75	1280x1024	VESA
1024x768	60.02(P)	75.00(P)	78.75	1280x1024	VESA
1024X768	60.24(N)	74.93(N)	80	1280x1024	Macintosh
1152x864	67.50(P)	75.00(P)	108	1280x1024	VESA
1152x870	68.68(N)	75.06(N)	100	1280x1024	Macintosh
1152x900	61.80(N)	66.00(N)	94.5	1280x1024	SUN 66
1152x900	71.81(N)	76.14(N)	108	1280x1024	SUN
1280x1024	64.00(P)	60.00(P)	108	1280x1024	VESA
1280x1024	75.83(N)	71.53(N)	128	1280x1024	IBM1
1280x1024	80.00(P)	75.00(P)	135	1280x1024	VESA
1280x1024	81.18(N)	76.16(N)	135.09	1280x1024	SPARC2

Note: "P", "N" stands for "Positive", "Negative" polarity of incoming H-sync/V-sync (input timing). For each timing detail, please refer to individual video signal standard.

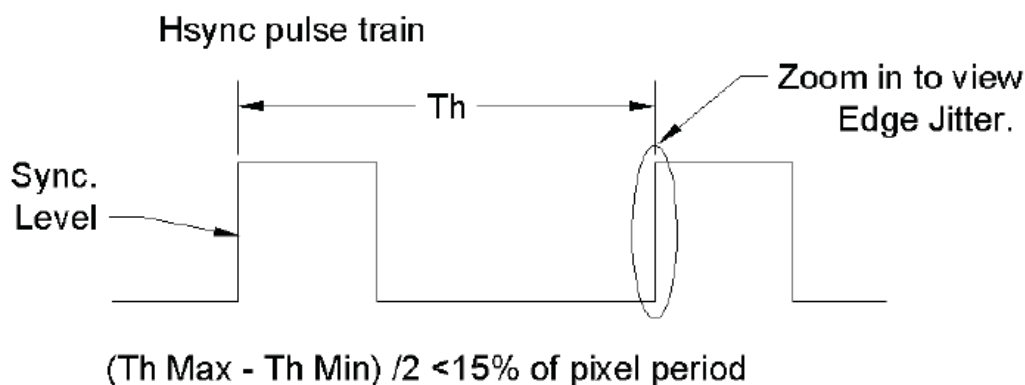
6.5.2 Definition of terms

➤ Video Signal Definition



- a) Vmin steady state Amplitude before transition
- b) Video Rise Time Delta (t), (measured from the 10% to 90% points of Vmin Steady State to Vmax Steady State)
- c) Overshoot Amplitude
- d) Undefined
- e) Settling Time - Measured from the end of the overshoot to the point where the amplitude of the video ringing is down to $\pm 5\%$ of the final steady state value
- f) Undefined
- g) Video Fall Time Delta (t), (measured from the 90% to 10% points of Vmax Steady State to Vmin Steady State)
- h) Undefined here, Note: Undershoot is within this period and with an Amplitude of (j)
- i) Settling Time - Measured from the end of the undershoot to the point where the amplitude of the video ringing is down to $\pm 5\%$ of the final steady state value
- j) Vmin steady state Amplitude after transition

➤ Synchronization Signal Definition





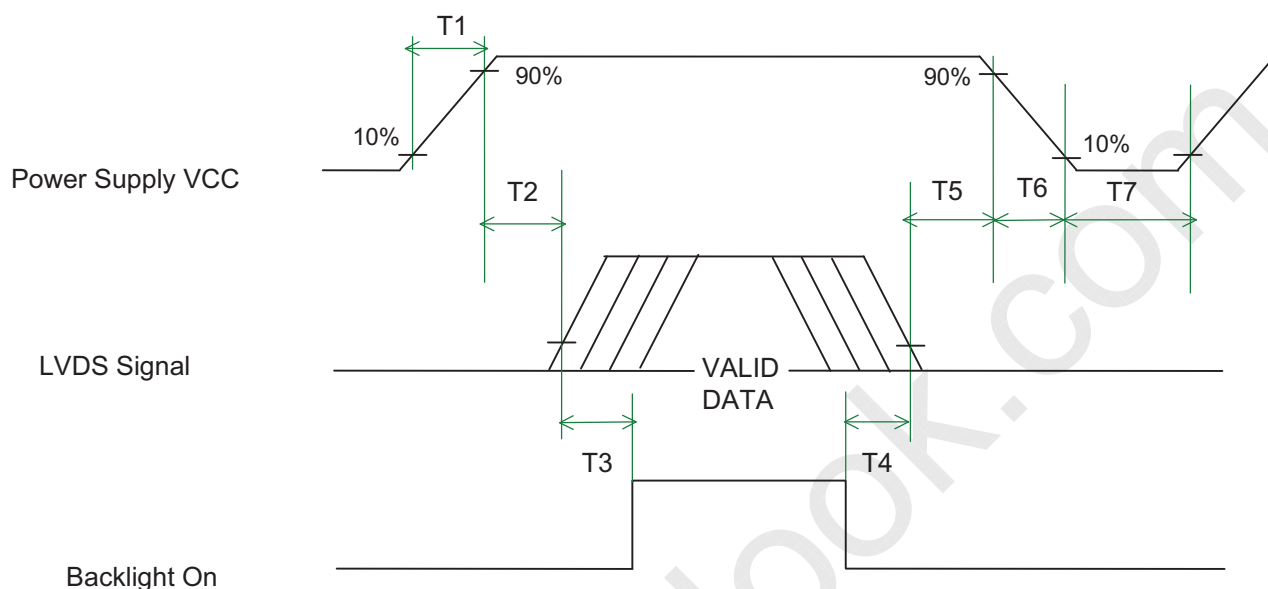
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6.6 Power ON/OFF Sequence

VCC power and lamp on/off sequence is as follows. Interface signals are also shown in the chart. Signals from any system shall be Hi-Z state or low level when VCC is off.



Power Sequence Timing

Parameter	Value			Unit
	Min.	Typ.	Max.	
T1	-	-	10	[ms]
10	50	-	10	[ms]
T3	200	-	-	[ms]
T4	100	-	-	[ms]
T5	0	16	50	[ms]
T6	-	-	50	[ms]
T7	1000	-	-	[ms]



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7. Connector & Pin Assignment

Physical interface is described as for the connector on module. These connectors are capable of accommodating the following signals and will be following components.

7.1 TFT LCD Module

7.1.1 Connector

Connector Name / Designation	Power Connector / J1
Manufacturer	STM or compatible
Type / Part Number	STM MS242612R
Mating Housing / Part Number	STM P242612

Connector Name / Designation	VGA Connector / J2
Manufacturer	STM or compatible
Type / Part Number	STM MS242614R
Mating Housing / Part Number	STM P242614R

Connector Name / Designation	OSD Connector / J4
Manufacturer	STM or compatible
Type / Part Number	STM MS242613R
Mating Housing / Part Number	STM PS242613

Connector Name / Designation	DVI Connector / J3
Manufacturer	STM or compatible
Type / Part Number	STM MDS240315
Mating Housing / Part Number	STM PDS240315

7.1.2 Pin Assignment



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➤ Power Connector (J1)

Pin#	Signal Name	Pin#	Signal Name
1	VCC	2	VCC
3	GND	4	GND
5	NC	6	GND
7	BKLT_ADJ	8	BKLT_EN
9	AUDIO_EN	10	MUTE ¹
11	VOLUME	12	GND

① Share with OSD source key

➤ VGA Connector (J2)

Pin#	Signal Name	Pin#	Signal Name
1	GND	2	VS
3	HS	4	GNDB
5	BIN	6	GNDG
7	GIN	8	GNDR
9	RIN	10	GND
11	SDA	12	SCL
13	PC5V	14	VGA_CON

➤ OSD Connector (J4)

Pin#	Signal Name	Pin#	Signal Name
1	GND	2	SOURCE
3	SELECT	4	LED_G
5	LED_A	6	UP
7	DOWN	8	MINUS
9	PLUS	10	MENU
11	Power	12	NC
13	GND		



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➤ DVI connector (J3)

Pin#	Signal Name	Pin#	Signal Name
1	GND	2	GND
3	RX2+	4	DVI_5V
5	RX2-	6	HPD
7	GND	8	GND
9	RX1+	10	SDA
11	RX1-	12	SCL
13	GND	14	GND
15	RX0+	16	NC
17	RX0-	18	NC
19	GND	20	GND
21	RXC+	22	DVI_CON
23	RXC-	24	GND
25	GND	26	NC
27	NC	28	GND
29	GND	30	NC



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7.2 Backlight Unit

Physical interface is described as for the connector on module. These connectors are capable of accommodating the following signals and will be following components.

Connector Name / Designation	Lamp Connector / Backlight Lamp
Manufacturer	JST
Type / Part Number	BHSR-02VS-1
Mating Type / Part Number	SM02(4.0)B-BHS-1-TB

7.2.1 Signal for Lamp connector

	Pin #	Cable color	Signal Name
Upper	1	Pink	High Voltage
	2	White	Low Voltage
	3	Pink	High Voltage
	4	White	Low Voltage

	Pin #	Cable color	Signal Name
Lower	1	Pink	High Voltage
	2	White	Low Voltage
	3	Pink	High Voltage
	4	White	Low Voltage



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8. Reliability Test

Environment test conditions are listed as following table.

Items	Required Condition	Note
Temperature Humidity Bias (THB)	Ta= 50℃, 80%RH, 300hours	
High Temperature Operation (HTO)	Ta= 50℃, 50%RH, 300hours	
Low Temperature Operation (LTO)	Ta= 0℃, 300hours	
High Temperature Storage (HTS)	Ta= 60℃, 300hours	
Low Temperature Storage (LTS)	Ta= -20℃, 300hours	
Vibration Test (Non-operation)	Acceleration: 1.5 G Wave: Random Frequency: 10 - 200 - 10 Hz Sweep: 30 Minutes each Axis (X, Y, Z)	
Shock Test (Non-operation)	Acceleration: 50 G Wave: Half-sine Active Time: 20 ms Direction: ±X, ±Y, ±Z (one time for each Axis)	
Drop Test	Height: 60 cm, package test	
Thermal Shock Test (TST)	-20℃/30min, 60℃/30min, 100 cycles	1
On/Off Test	On/10sec, Off/10sec, 30,000 cycles	
ESD (ElectroStatic Discharge)	Contact Discharge: ± 8KV, 150pF(330Ω) 1sec, 8 points, 25 times/ point.	2
	Air Discharge: ± 15KV, 150pF(330Ω) 1sec 8 points, 25 times/ point.	
Altitude Test	Operation:10,000 ft Non-Operation:30,000 ft	

Note 1: The TFT-LCD module will not sustain damage after being subjected to 100 cycles of rapid temperature change. A cycle of rapid temperature change consists of varying the temperature from -20℃ to 60℃, and back again. Power is not applied during the test. After temperature cycling, the unit is placed in normal room ambient for at least 4 hours before power on.

Note 2: According to EN61000-4-2 , ESD class B: Some performance degradation allowed. No data lost. Self-recoverable. No hardware failures.



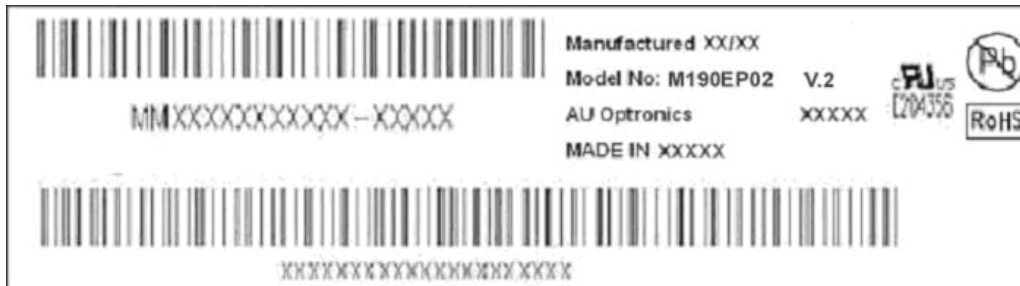
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9. Shipping Label

The shipping label format is shown as below.



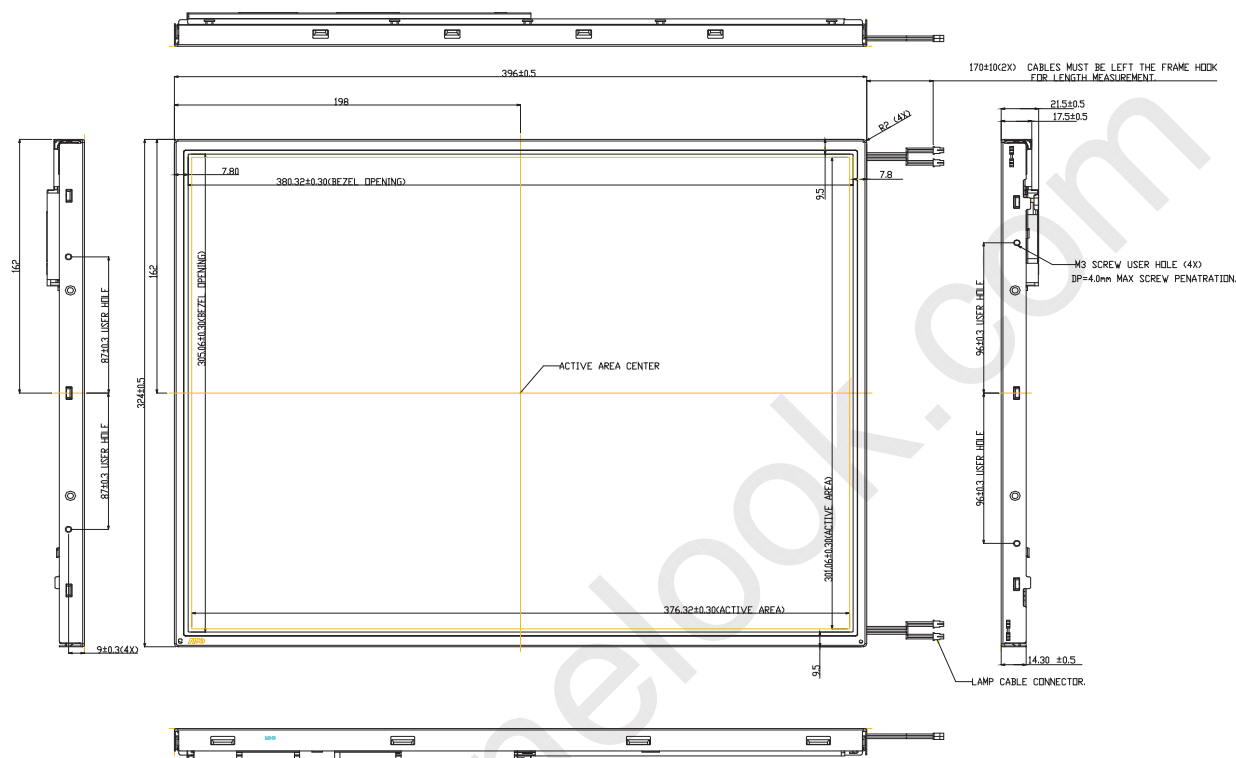


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10. Mechanical Characteristics

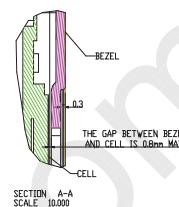
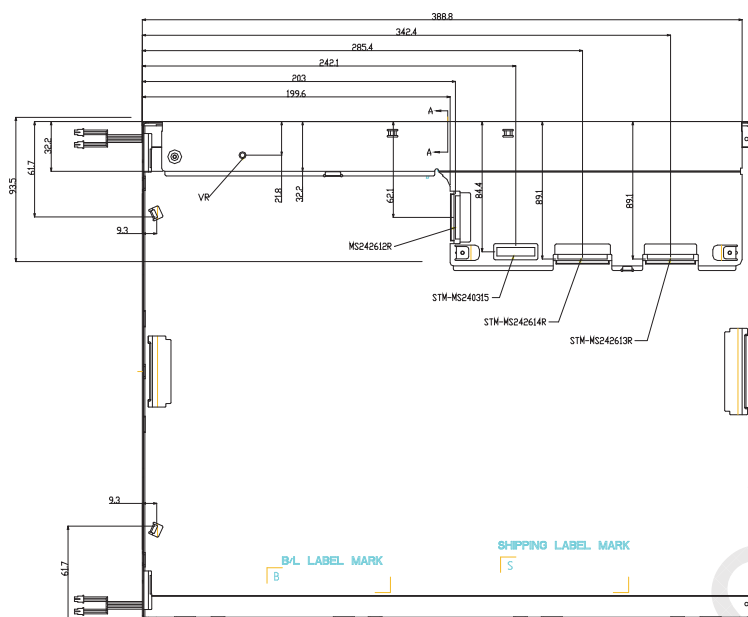




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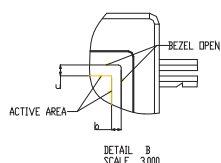
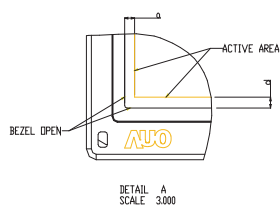




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NOTE:
1. PRELIMINARY DRAWING FOR REFERENCE ONLY.
2. THE DIMENSION EXCLUDES DEFORMATION.
3. MODULE THICKNESS SHOULD BE 22mm MAX.
4. UNSPECIFIED TOLERANCE MUST FOLLOW TOLERANCE TABLE.
5. SLAMP CABLE CONNECTOR TO BE JST BSHR-02VS-1
6. I/F CONNECTOR TO BE JAE FT-XB30SL-HF15
7. M3 USER HOLE SCREW TORQUE 4.0kgf-cm MAX.
8. USER HOLE SCREW PENETRATION 4.0mm MAX.
9. DIMENSION TOLERANCE: 10-40 ± 0.10 40-80 ± 0.15 80-100 ± 0.20
10. CABLE LENGTH IS 170±10.0mm FROM THE END OF HI-VOLTAGE.

